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EXAMINER	
NGUYEN, TOAN D	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/988,940	KENDALL ET AL.	
	Examiner	Art Unit	
	Toan D. Nguyen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12,14-18,20-22 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 18* is/are allowed.

6)☒ Claim(s) *1,3-10,12,14-17,20-22 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-10, 12, 14-17, 20-22, 24-25, and 27-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delvaux (US 6,775,305) in view of Vallee et al. (WO 96/17489).

For claims 1, 4, 33, 34 and 38, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

a first demultiplexer (figure 8, reference 144a) for dividing data packets of a high-rate data stream into data stream into N sub-streams (figure 8, references 143_0-143_N, col. 16 lines 61-64), so that each sub-stream carries every N^{th} data packet of the high-rate data stream (figure 11, reference step 212, col. 20 lines 18-20) and data packets in the N sub-stream are staggered in time with respect to one another (figure 9, references line 0 and line 1, col. 18 lines 53-65);

a plurality of data transmitting devices (figure 8, references 143_0-143_N), each data transmitting device (figure 8, reference 143) associated with a corresponding on of the N sub-streams for serializing data from the corresponding one of the N sub-streams and transmitting the serialized data via a corresponding first serial data connection over

said mid-plane (figure 8, reference 146) to a data receive interface (figure 8, reference 145)(col. 18 lines 28-30).

However, Delvaux does not expressly disclose:

a first transmit control circuit connected to the data transmitting devices and configured:

to insert flow control signals into one or more of the N sub-streams, and

to selectively enable and disable the data transmitting device in response to first receiver enable signals received over said mid-plane from the data receive interface,

whereby packet integrity and sequencing is maintained at said data transmission apparatus.

In an analogous art, Vallee et al. disclose:

a first transmit control circuit connected to the data transmitting devices (figure 8, reference AIM) and configured:

to insert flow control signals into one or more of the N sub-streams (page 8, lines 26-35), and

to selectively enable and disable the data transmitting device in response to first receiver enable signals received over said mid-plane from the data receive interface (page 6, lines 15-28, and page 8 line 32 to page 9 line 20),

whereby packet integrity and sequencing is maintained at said data transmission apparatus (page 8 lines 26-35).

Vallee et al. disclose wherein the first receive control circuit is configured to provide the first receiver enable signals to the first transmit control circuit in response to

a status of at least one of the plurality of buffers (page 6 lines 15-28 as set forth in claim 4); for altering the first receiver enable signals based on a status of at least one of the plurality of buffers (page 9, lines 11-15 as set forth in claim 33), means for generating a first receiver enable signal which cause the first transmit control circuit to disable at least one of the data transmitting devices upon arrival, in one of the plurality of buffers, of a second last packet that the one of the plurality of buffers can hold (page 6 lines 19-28, and page 9 lines 11-15 as set forth in claim 34), wherein the first receive control circuit is configured to provide the flow control signals to the first transmit control circuit in response to a status of at least one of the plurality of buffers and the flow control signals, when received at the data receive interface over the first serial data connections, cause the data receive interface to inhibit transmission of at least one of the corresponding sub-streams of data over the mid-plane via the corresponding second serial connections (page 9 lines 11-15 as set forth in claim 38).

One skilled in the art would have recognized the first transmit control circuit connected to the data transmitting devices, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to provide the feedback link status which is made available for the receiver to inform the transmitter, by sending its own SN cells, that it is receiving cells and it is also an integral part of the same round robin

mechanism, that is to say, the feedback link status SN cells in either direction must agree with each other (page 6, lines 19-28).

For claim 3, Delvaux discloses:

a plurality of data receive devices (figure 8, reference 145, col. 16 lines 17-18), each data receive device connected to receive a corresponding sub-stream of data comprising data transmitted by one of the data transmitting device (figure 8, reference 143) over the mid-plane via a corresponding one of the first serial connections (col. 18 lines 28-30);

a plurality of buffers (figure 8, reference 142b), each buffer associated with a corresponding one of the data receive devices (figure 8, reference 145) and configured to receive fixed-length data packets carried in the corresponding sub-stream (col. 16 lines 19-36), and

a first receive control circuit configured to determine a sequence of arrival of the fixed length data cells at the plurality of buffers (col. 17 lines 25-31).

For claim 5, Delvaux discloses wherein the first receive control circuit is configured to demultiplex the flow control signals from the one or more of the N sub-streams (col. 17 lines 25-31).

For claim 6, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

a first demultiplexer (figure 8, reference 144a, col. 16 lines 14-15) connected to receive the data stream and to split the data stream by delivering the transmit packets in rotation into a plurality of N transmit channels (figure 8, references 143_0-143_N, col. 16

lines 61-64), so that each transmit channel carries every N^{th} transmit packet (col. 2 lines 42-45);

a plurality of data transmitting devices (figure 8, reference 143), each data transmitting device connected to receive the transmit packets of a corresponding one of the N transmit channels (figure 8, reference 146) and to output the transmit packets of the corresponding one of the N transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprise a serial data connection (figure 8, reference 144b)(col. 16 line 61 to col. 17 line 3, and col. 18 lines 28-30);

the apparatus comprising:

a first receive interface (figure 8, reference 145, col. 17 lines 25-28) comprising:

a plurality of deserializer devices, each of the deserializer devices connected for receiving a corresponding serial stream of receive packets received over the mid-plane from the receiver in a corresponding receive channel (col. 17 lines 25-28);

a plurality of buffers (figure 8, reference 142b), each of the buffers connected to accept the receive packets from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the receive packets (col. 16 lines 19-36);

a first receive control circuit configured to determine a sequence of arrival

of the receive packets in the plurality of buffers and to place the receive cells onto a bus in the sequence of arrival (col. 17 lines 25-31).

However, Delvaux does not expressly disclose:

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit packets in sequence with commencement of transmission of the transmit packets from sequential data transmitting devices staggered in time relative to one another by a time difference T; and

wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q cells, with Q 1 and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit packets to the receiver.

In an analogous art, Vallee et al. disclose:

a first transmit control circuit connected to the data transmitting devices (figure 8, reference AIM), the first transmit control circuit configured to cause the data transmitting devices to output the transmit cells in sequence with commencement of transmission of the transmit packets from sequential data transmitting devices staggered in time relative to one another by a time difference T (page 8, lines 26-35); and

wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q packets, with Q 1 and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit packets to the receiver (page 6, lines 19-28).

One skilled in the art would have recognized the first transmit control circuit connected to the data transmitting devices, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to provide the feedback link status which is made available for the receiver to inform the transmitter, by sending its own SN cells, that it is receiving cells and it is also an integral part of the same round robin mechanism, that is to say, the feedback link status SN cells in either direction must agree with each other (page 6, lines 19-28).

For claim 7, Delvaux et al. discloses wherein the first transmit control circuit is configured to multiplex the flow control signal with the transmit packets in one of the transmit channels (col. 16 line 62 to col. 17 line 3).

For claims 8 and 10, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

a first demultiplexer (figure 8, reference 144a, col. 16 lines 14-15) connected to receive the data stream and to split the data stream by delivering the packets in rotation into a plurality of N transmit channels (figure 8, references 143_0-143_N, col. 16 lines 61-64) so that each transmit channel carries every N^{th} transmit cell (col. 2 lines 42-45),

a plurality of data transmitting devices (figure 8, reference 143), each data transmitting device connected to receive the transmit packets of a corresponding one of the N transmit channels (figure 8, reference 146) and to output the transmit packets of

the corresponding one of the N transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprise a serial data connection (figure 8, reference 144b)(col. 16 line 61 to col. 17 line 3, and col. 18 lines 28-30); and

wherein the first transmit interface is located on a line card of the network element (figure 8, reference 143) having an interface for receiving the data stream, the receiver on a second card of the network element (figure 8, reference 145), and the serial data connections comprise data lines extending between the line card and the second line card through a midplane of the network element (figure 8, reference 146)(col. 16 lines 62-64 and col. 18 lines 28-30).

However, Delvaux does not expressly disclose:

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit packets in sequence with commencement of transmission of the transmit packets from sequential data transmitting devices staggered in time relative to one another by a time difference T.

In an analogous art, Vallee et al. disclose:

a first transmit control circuit connected to the data transmitting devices (figure 8, reference AIM), the first transmit control circuit configured to cause the data transmitting devices to output the transmit cells in sequence with commencement of transmission of

the transmit packets from sequential data transmitting devices staggered in time relative to one another by a time difference T (page 8, lines 26-35).

Vallee et al. disclose wherein the second receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q cells or fewer, with Q 1, wherein the second card comprises a transmitter connected to transmit the flow control signal to the line card and wherein the first transmit control circuit is configured, in response to the flow control signal, to inhibit transmission of the transmit packets on at least one of the N transmit channels corresponding to the one of the buffers which has the remaining capacity of Q packets or fewer (page 8, lines 26-35 as set forth in claim 10).

One skilled in the art would have recognized the first transmit control circuit connected to the data transmitting devices, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to provide the feedback link status which is made available for the receiver to inform the transmitter, by sending its own SN cells, that it is receiving cells and it is also an integral part of the same round robin mechanism, that is to say, the feedback link status SN cells in either direction must agree with each other (page 6, lines 19-28).

For claim 9, Delvaux discloses wherein the receiver comprises a second receive interface, the second receive interface comprising:

a plurality of deserializer devices, each of the deserializer devices connected to corresponding one of the data connections for receiving the transmit packets of the corresponding one of the N transmit channels after transmission of the transmit packets of the corresponding one of the N transmit channels from the line card to the second card over the mid-plane (col. 17 lines 25-28);

plurality of buffers, each of the buffers connected to accept the transmit packets from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the transmit packets (col. 16 lines 19-36); and

a second receive control circuit configured to determine a sequence of arrival of the transmit packets in the serial data in the plurality of buffers and to place the transmit packets onto a bus in the sequence of arrival (col. 17 lines 25-31).

For claim 12, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

a) means for carrying a data stream comprising a sequence of packets having an order (figure 8, col. 16 lines 37-60);

b) demultiplexing means (figure 8, reference 144a) for assigning each of the packets of the data stream to one of a plurality of channels (figure 8, reference 143) (col. 16 line 61 to col. 17 line 3);

c) transmitting means for transmitting the packets in each channel to a receiver by way of signal conductors in a mid-plane (figure 8, reference 146) (figure 8, reference 144b)(col. 17 lines 25-28 and col. 18 lines 28-29);

e) receiving the packets in the order at the receiver (col. 17 lines 25-31).

However, Delvaux does not expressly disclose:

d) control means for commencing the transmission of individual packets to the receiver, in the order, at times staggered relative to one another by a time difference T that exceeds a worst case interchannel difference in latency for transmission of packets from the transmitting means to the receiver.

In an analogous art, Vallee et al. disclose:

d) control means for commencing the transmission of individual packets to the receiver, in the order, at times staggered relative to one another by a time difference T that exceeds a worst case interchannel difference in latency for transmission of packets from the transmitting means to the receiver (page 8, lines 26-35).

One skilled in the art would have recognized the control means for commencing the transmission of individual packets to the receiver, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to readjust the differential delays among link (page 9 line 25).

For claim 14, Delvaux discloses means for receiving a plurality of serially transmitted packets in a plurality of channels and means for determining an order of arrival of the plurality of packets (figure 8, col. 16 line 49 to col. 17 line 28).

For claim 15, Delvaux discloses a first receive interface for receiving a data stream, the first receive interface comprising a plurality of receiving devices each for

receiving a stream of packets in one of a plurality of channels (figure 8, col. 16 line 49 to col. 17 line 28), and a first receive control circuit configured to determine a sequence of arrival of the packets and to place the packets onto a bus in the sequence of arrival (col. 17 lines 25-31).

For claim 16, Delvaux discloses wherein the first receive interface is adapted to receive in the data stream a first direction flow control signal and the first transmit control circuit is connected to receive the flow control signal and adapted to selectively enable or inhibit the transmission of packets by one of the data transmission devices in response to the flow control signal (col. 17 lines 25-28).

For claim 17, Delvaux discloses wherein the first receive interface is adapted to generate a second direction flow control signal and the first transmit control circuit is adapted to cause one of the data transmitting devices to output the second direction flow control signal (col. 17 lines 25-28).

For claims 20, Delvaux discloses comprising serializing the data on each of the channels before transmitting the data on each of the channels (figure 8, reference 143)(col. 16 line 61 to col. 17 line 3).

For claim 21, Delvaux discloses wherein there are N channels and assigning the consecutive packets of the data stream into different ones of the plurality of channels comprises assigning the consecutive packets to the channels in rotation so that each channel carries every Nth packet (col. 2 lines 42-45).

For claim 22, Delvaux discloses wherein transmitting the data on each of the channels comprises transmitting a plurality of streams of serial data (figure 8, col. 16 lines 49-64).

For claims 24 and 29, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

assigning consecutive packets of the data stream into different ones of a plurality of channels (figure 8, reference 146)(col. 16 line 61 to col. 17 line 8).

However, Delvaux does not expressly disclose:

simultaneously transmitting data on each of the channels from the transmitter to the receiver while staggering commencement of transmission of the packets assigned to each channel in time relative to one another by a time difference T;

inhibiting transmission of cells in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver;

upon inhibiting transmission of packets in the at least one of the channels;

waiting without transmission of packets in the at least one of the channels; and

after waiting, recommencing transmission of packets in the at least one of the channels an inter multiple of the time difference T after a time at which transmission of a previous packet commenced on the at least one of the channels.

In an analogous art, Vallee et al. disclose:

simultaneously transmitting data on each of the channels from the transmitter (figure 8, reference 22) to the receiver (figure 8, reference 28) while staggering

commencement of transmission of the packets assigned to each channel in time relative to one another by a time difference T (page 8, lines 26-35);

inhibiting transmission of packets in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver (page 9 lines 11-15);

upon inhibiting transmission of packets in the at least one of the channels (page 9, lines 11-15);

waiting without transmission of packets in the at least one of the channels (page 9, lines 11-15); and

after waiting, recommencing transmission of packets in the at least one of the channels an inter multiple of the time difference T after a time at which transmission of a previous packet commenced on the at least one of the channels (page 9, lines 16-20).

Vallee et al. disclose wherein for each channel, suspending transmission of packets on the channel comprises issuing a first flow control signal corresponding to the channel and sending the first flow control signal corresponding to the channel from the receiver to the transmitter (page 9 lines 11-15 as set forth in claim 29).

One skilled in the art would have recognized the simultaneously transmitting data on each of the channels from the transmitter to the receiver while staggering commencement of transmission of the packets assigned to each channel in time relative to one another by a time difference T, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM

inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to readjust the differential delays among link (page 9 line 25).

For claim 25, Delvaux discloses for at least one channel, multiplexing a second flow control signal with the data on each of the channels and before transmitting the data on each of the channels (figure 8, col. 16 lines 61-64).

For claim 27, Delvaux discloses receiving the data on each of the channels at the receiver, deserializing the received data, identifying an order of arrival of received packets at the receiver and placing the received packets on a signal bus in their order of arrival (col. 17 lines 25-28).

For claim 28, Delvaux discloses for each channel, monitoring a number of the received packets which have arrived at the receiver and have not yet been placed on the signal bus; and suspending transmission of packets on the channel if the number exceeds a threshold (col. 20 lines 30-32).

For claims 30, Delvaux discloses system and method for combining multiple physical layer transport links, comprising:

assigning each of the packets in the sequence to one of a plurality of channels (figure 8, reference 143), each of the channels having a recurring packet transmit time (col. 16 lines 52-64);

in each of the channels (figure 8, reference 143), transmitting the packets in the sequence in order of the sequence from the transmitting device to the receiving device over one or more serial data connections (figure 8, reference 145) and commencing

transmission of each packet assigned to the channel only at the cell transmit time for that channel (col. 17 lines 9-31 and col. 18 lines 28-30); and

receiving transmitted packets at the receiving device in the same order that the transmitted packets were transmitted from the transmitting device (col. 17 lines 25-31).

However, Delvaux does not expressly disclose the packet transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency. In an analogous art, Vallee et al. disclose the packet transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency (page 8, lines 26-35).

One skilled in the art would have recognized the packet transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency, and would have applied Vallee et al.'s AIM in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Vallee et al.'s ATM inverse multiplexing in Delvaux's system and method for combining multiple physical layer transport links with the motivation being to readjust the differential delays among link (page 9 line 25).

For claim 31, Delvaux discloses deserializing the transmitted packets at the receiving device, and detecting an order of arrival of the transmitted packets at the receiving device (col. 17 lines 25-31).

For claim 32, Delvaux discloses receiving a plurality of packets in the sequence substantially simultaneously at the transmitting device and assigning each of the plurality of packets in the sequence to one of the plurality of channels in rotation (col. 2 lines 42-45).

For claim 35, Delvaux discloses wherein the sub-streams are staggered in time by T, and T is greater than a maximum total skew due to the mid-plane, the data transmitting device and the data receive interface (col. 19 lines 10-15).

For claim 36, Delvaux discloses wherein the flow control signals comprise a clock signal, a parity signal, and a start of cell signal (col. 8 line 43).

For claim 37, Delvaux discloses comprising:

a plurality of data receive devices (figure 8, reference 145, col. 16 lines 17-18), each data receive device connected to receive a corresponding sub-stream of data comprising data transmitted from the data receive interface over the mid-plane via a corresponding second serial connection (col. 18 lines 28-30);

a plurality of buffers (figure 8, reference 142b), each buffer associated with a corresponding one of the data receive devices (figure 8, reference 145) and configured to receive fixed-length data packets carried in the corresponding sub-stream (col. 16 lines 19-36), and

a first receive control circuit configured to determine a sequence of arrival of the fixed-length data packets at the plurality of buffers (col. 17 lines 25-31).

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delvaux (US 6,775,305) in view of Vallee et al. (WO 96/17489) further in view of McKeown et al. (US 6,647,019).

For claim 26, Delvaux in view of Vallee et al. does not expressly disclose wherein the sequence of packets comprises an OC-192 data stream. In an analogous art, McKeown et al. disclose wherein the sequence of packets comprises an OC-192 data stream (col. 8 lines 66-67).

One skilled in the art would have recognized the OC-192 data stream, and would have applied McKeown et al.'s line card in Delvaux's multi-channel communication link. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use McKeown et al.'s packet-switch system in Delvaux's system and method for combining multiple physical layer transport links with the motivation being received an ATM cell from an external OC-192 line (col. 8 lines 66-67).

Allowable Subject Matter

4. Claims 11 and 18 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 11, the prior art fails to teach a combination of the steps of:

the transmitter on the second card comprises a second transmit interface for transmitting a second data stream comprising a second sequence of fixed-size second packets to the line card, the second transmit interface comprising:

a second demultiplexer connected to receive the second data stream and to split the second data stream by delivering the second cells in rotation into a second plurality

of N second channels so that each said second channel carries every Nth second packet;

a plurality of second serializer devices, each second serializer device connected to receive the second packets of a corresponding one of the N second channels and to output the second cells as serial data on one or more second serial data connections over the mid-plane to the line card; and.

a second transmit control circuit connected to the second serializer devices, the second transmit control circuit configured to cause the second serializer devices to output the second packets of the second data stream in sequence and staggered in time relative to one another by a time difference T, in the specific combination as recited in the claim.

Regarding claim 18, the prior art fails to teach a combination of the steps of:

for each second direction channel a serializer device connected to receive the packets of the second direction channel and to output the packets as serial data on one or more serial data connections extending through the midplane to the line card;

a second transmit control circuit connected to the serializer devices, the transmit control circuit configured to cause the serializer devices to output the packets in sequence order with the commencement of transmission of packets on different second direction channels staggered in time relative to one another by a time difference T;

a plurality of second deserializer devices at the line card, the deserializer devices connected to receive and deserialize the serial data on the serial data connections; and

a second direction receive control circuit connected to detect an order of arrival of packets on the serial data connections and to place the packets into a received data stream in the order of arrival, in the specific combination as recited in the claim.

Response to Arguments

5. Applicant's arguments filed 02/05/07 have been fully considered but they are not persuasive.

The applicant argues with respect to claim 1, on page 23, second paragraph, that Delvaux fails to teach or suggest "each substream carries every Nth data packet" as recited in claim 1. The examiner disagrees. Applicant's attention is directed to Delvaux patent at col. 20 lines 18-20 (see figure 11, reference step 212), where Delvaux clearly teaches "...by performing step 212 where ATM cell N is transferred to the appropriate physical transport medium (each substream carries every Nth data packet means)." The applicant further argues that Delvaux fails to disclose the claim 1 feature that the data packets in the N sub-streams are "staggered in time with respect to one another". The examiner disagrees. Delvaux clearly teaches at col. 18 lines 53-65 (see figure 9), "The transmit timing diagram 160 reveals the relative cell position in time of each of the seven ATM cells ...", and Delvaux teaches further at col. 19 lines 3-6, "A strict round robin operation would send cell 1 163_1 as cell 163 (the first cell on line 0), as cell 1 163_1 is ready for transport before the cell transport opportunity on line 0 as represent by the dummy cell 163." (the data packets in the N sub-streams are "staggered in time with respect to one another" means).

On page 24, first paragraph, the applicant argues that Delvaux does not disclose serialized data transmission between a data transmitting device and a data receive interface over a pin-limited mid-plane as recited in claim 1. The examiner disagrees. In claim 1, the limitation "over a pin-limited mid-plane" is not disclosed. Therefore, Delvaux does teach serialized data transmission between a data transmitting device and a data receive interface over said mid-plane as recited in claim 1 (see page 3, second paragraph of Office action).

With respect to claims 6 and 7, the applicant argues on page 24, fourth paragraph, that Delvaux does not disclose that each of N transmit channels carries every Nth transmit packet as recited in claim 6. The applicant further argues on page 25, fourth paragraph, that Delvaux does not disclose the claim 6 combination of "a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit in sequence with commencement of transmission of the transmit from sequential data transmitting devices staged in time relative to one another by a time difference T" and "wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q, with Q>1 and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit to receiver." The examiner disagrees. The examiner refers to the same response to claim 1 above, and the Office action page 8, first and second paragraphs.

The applicant argues with respect to claims 8-10, 12 and 14-17, 20-22 and 24-29, and 30-32, that Delvaux does not disclose or suggest that each of N transmit

channels carries every Nth transmit packet as recited in claim 8. Delvaux does not teach or suggest transmission of packets over a mid-plane as recited in claim 12.The examiner disagrees. The examiner refers to the Office action page 9 for claims 8 and 10), page 11 for claim 12, page 14 for claims 20-22, and 24-29, and page 16 for claims 30-32.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D. Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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